IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Adrianus Josephus Bink et al. Group Art Unit: 2185

Application No.: 10/570,290 Examiner: Giardino Jr., Mark A.

Filed: February 28, 2006 Confirmation No.: 5446

For: INTEGRATED CIRCUIT AND A METHOD OF CACHE REMAPPING

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated February 27, 2009, which finally rejected claims 1-20 in the above-identified application. The Office date of receipt of Appellants' Notice of Appeal was May 27, 2009. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

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Date:_____ Signed:_____

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, NXP B.V., of Eindhoven, Netherlands.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF CLAIMS

No claims are canceled.

No claims are withdrawn.

No claims are objected to.

Claims 1-20 stand rejected as follows:

Claims 1, 2, 4, 5, 7, 8, 13, 14, and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Cherabuddi (U.S. Pat. No. 6,725,336, hereinafter Cherabuddi).

Claims 3, 9-11, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherabuddi in view of Asher (U.S. Pat. No. 6,671,822, hereinafter Asher).

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherabuddi in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer).

Claims 12, 16, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherabuddi in view of Supnik (U.S. Pat. No. 5,070,502, hereinafter Supnik).

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherabuddi in view of Emma (U.S. Pat. No. 5,584,002, hereinafter Emma).

Claims 1-20 are the subject of this appeal. A copy of claims 1-20 is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

There were no proposed amendments submitted subsequent to the Final Office Action mailed February 27, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This section of this Appeal Brief is set forth to comply with the requirements of 37 C.F.R. § 41.37(c)(1)(v) and is not intended to limit the scope of the claims in any way. Examples of implementations of the limitations of independent claims 1 and 8 are described below.

The language of claim 1 relates to an integrated circuit. In one embodiment, the integrated circuit includes an at least one processing unit. Detailed Description, page 5, lines 3-11; Fig. 1, processing units TM. The integrated circuit also includes a cache memory which has a plurality of memory modules for caching data. Detailed Description, page 5, lines 3-11; Fig. 1, cache L2 bank. The cache memory comprises a plurality of distinct physical banks. Detailed Description, page 5, lines 12-20; Fig.1 cache L2 bank. Each physical bank includes some of the memory modules and facilitates serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks. Detailed Description, page 5, lines 12-20. The integrated circuit also includes remapping means for performing an unrestricted remapping within the plurality of memory modules. Detailed Description, page 6, line 10, through page 7, line 2; Fig. 3, remapping means RM. Examples of structures corresponding to the remapping means are the remapping means RM of Fig. 3 and the MapRAM of Fig. 4, although other structures may correspond to the remapping means in addition to or instead of these structures. The unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules. Detailed Description, page 5, lines 24-28; Fig. 2, remapping arrows.

The language of claim 8 relates to a method of cache remapping in an integrated circuit having at least one processing unit; a main memory for storing data; and a cache memory having a plurality of memory modules for caching data. Detailed Description,

page 5, lines 3-11. The method includes performing an unrestricted remapping within the plurality of memory modules. Detailed Description, page 5, line 29, through page 6, line 2; Fig. 2, remapping arrows. The memory modules are distributed among a plurality of distinct physical banks within the cache memory. Detailed Description, page 5, line 29, through page 6, line 2; Fig. 2. Each physical bank is configured to facilitate serving a read/write request independently of the other physical bands to allow concurrent transfers for at least two of the physical banks. Detailed Description, page 5, lines 12-20. The unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of modules. Detailed Description, page 5, lines 24-28; Fig. 2, remapping arrows.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1, 2, 4, 5, 8, and 14 are patentable over Cherabuddi under 35 U.S.C. § 102(b).

B. Whether claim 7 is patentable over Cherabuddi under 35 U.S.C. § 102(b).

C. Whether claims 13 and 17 are patentable over Cherabuddi under 35 U.S.C. § 102(b).

D. Whether claims 11 and 18 are patentable over the combination of Cherabuddi and Asher under 35 U.S.C. § 103(a).

E. Whether claims 3, 9, and 10 are patentable over the combination of Cherabuddi and Asher under 35 U.S.C. § 103(a).

F. Whether claim 6 is patentable over the combination of Cherabuddi and Kramer under 35 U.S.C. § 103(a).

G. Whether claims 12, 16, 19, and 20 are patentable over the combination of Cherabuddi and Supnik under 35 U.S.C. § 103(a).

H. Whether claim 15 is patentable over the combination of Cherabuddi and Emma under 35 U.S.C. § 103(a).

VII. ARGUMENT

For the purposes of this appeal, claims 1, 2, 4, 5, 7, 8, and 14 are argued together as a group for purposes of the question of patentability over Cherabuddi under § 102(b). Claims 13 and 17 are argued together as a separate group for purposes of the question of patentability over Cherabuddi under § 102(b). Claim 9 is argued separately for purposes of the question of patentability over the combination of Cherabuddi and Asher under § 103(a). Claims 11 and 18 are argued separately for purposes of the question of patentability over the combination of Cherabuddi and Asher under § 103(a). Claims 3 and 10 are argued separately for purposes of the question of patentability over the combination of Cherabuddi and Asher under § 103(a). Claim 6 is argued separately for purposes of the question of patentability over the combination of Cherabuddi and Kramer under § 103(a). Claims 12, 16, 19, and 20 are argued as a separate group for purposes of the question of patentability over the combination of Cherabuddi and Supnik under § 103(a). Claim 15 is argued separately for purposes of the question of patentability over the combination of Cherabuddi and Emma under § 103(a).

A. Claims 1, 2, 4, 5, 7, 8, and 14 are patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims.

Appellants respectfully submit that claim 1 is patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claim. Claim 1 recites:

> An integrated circuit, comprising:
>
> at least one processing unit (PU);
>
> a cache memory (L2_bank) having a plurality of memory modules for caching data, wherein the cache memory comprises a plurality of distinct physical banks, wherein each physical bank comprises some of the memory modules and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks;
>
> remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules.
>
> (Emphasis added.)

In contrast, Cherabuddi does not disclose all of the limitations of the claim because Cherabuddi does not disclose remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules, as recited in the claim. In fact, the Examiner recognizes that Cherabuddi does not explicitly disclose the indicated limitations. The Examiner recognizes this lack of explicit disclosure by Cherabuddi because the Examiner asserts that it is allegedly inherent in Cherabuddi to remap memory modules between first and physical banks. However, this assertion of inherency is insufficient to support the rejection of claim 1 at least because the assertion of inherency is not properly supported by rationale or evidence, as required by the MPEP. Consequently, the rejection based on the purportedly inherent disclosure of Cherabuddi is improper because the Examiner fails to establish a proper showing of inherency. Moreover, Cherabuddi does not inherently disclose the indicated limitations.

1. The Examiner's reliance on inherency is improper because the Examiner fails to provide rationale or evidence in support of the asserted inherency.

The Examiner's position in the Advisory Action mailed May 13, 2009, is inconsistent with the explicit statement made by the Examiner in the Office Action mailed February 27, 2009. In the Advisory Action, the Examiner states "The only limitations asserted as inherent in the Office Action are the presence of memory modules within the cache and the division of cache memory, made up of SRAM, into physical banks." Advisory Action, 5/13/09, page 2, lines 4-6 (emphasis added). This statement clearly excludes the remapping means which are not listed as being subject to the assertions of inherency. However, the Office Action explicitly states "a processor may use "both the first and second cache memory partitions", thus remapping means are inherently present to remap the partition 23b of Figure 2 [used for the second processor in a different mode [to join the partition of the first processor" Office Action, 2/27/09, page 3, lines 16-18 (emphasis added). Thus, there is an inconsistency between the Examiner's statements regarding the reliance on inherency in the Office Action and in the Advisory Action. To the extent that the Examiner relies on inherency to show the purported disclosure of remapping means as recited in the claim, the reliance on inherency is

improper because it is not properly supported by rationale or evidence, as required in the MPEP.

The MPEP states that the Examiner must provide rationale or evidence in order to show inherency. MPEP 2112(IV). More specifically, " '[i]n relying on a theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the assertion that an allegedly inherent characteristic necessarily flows from the teachings of the cited reference.' " Id. (quoting *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (first emphasis added)). Moreover, the MPEP states that the possible occurrence of a result or characteristic is not sufficient to establish inherency of the asserted result or characteristic. Id. ("The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." (emphasis in original) (citing *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993)); "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " (quoting *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted)).

The conclusion of inherency asserted by the Examiner in the Office Action regarding the remapping means is improper because it is not supported by any rationale or evidence. In the Office Action, the Examiner merely restates some of the disclosure of Cherabuddi related to allocating different cache memory partitions to different active processors. However, the referenced portions of Cherabuddi do not provide rationale or evidence in support of the assertion of inherency because the cited portions of Cherabuddi do not relate to remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules.

For reference, Cherabuddi generally describes a multiprocessor computer system which includes multiple processors and a shared cache memory. Cherabuddi, abstract. The cache memory is partitioned into first and second cache memory partitions. Cherabuddi, col. 3, lines 31-34. A cache access circuit dynamically allocates the cache

resources (i.e., the first and second cache memory partitions) between the first and second processors according to each processor's processing requirements. Cherabuddi, col. 3, lines 42-46. For example, if both processors are active, then the cache access circuit allows each processor to use a corresponding cache memory partition as dedicated cache. Cherabuddi, col. 2, lines 7-12. As another example, if only one processor is active, then the cache access circuit allows the active processor to use both the first and second cache memory partitions. Cherabuddi, col. 2, lines 25-29. Thus, Cherabuddi merely describes allocating cache memory partitions between multiple processors. However, Cherabuddi does not address remapping memory modules between different physical banks of memory.

Although the Examiner concludes in the Office Action that remapping memory modules between different physical banks of memory is allegedly inherent, based on the description of dynamically allocating different cache memory partitions to different active processors, the Examiner does not attempt in the Office Action to provide any rationale to explain why or how remapping memory modules between different physical banks of memory might be inherent. More specifically, the Examiner does not attempt in the Office Action to explain how the disclosure of allocating different cache memory partitions to different processors (or to the same processor), generally, necessarily would lead to the asserted conclusion of inherency regarding remapping memory modules between different physical banks of memory. In fact, there is no mapping between different physical banks of memory, or from one physical bank to another, because Cherabuddi merely addresses which processors are capable of accessing all of part of the cache. And even if assigning different portions of the cache to one or more processors were considered some type of mapping event, such processor mapping nevertheless is insufficient to address remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules, at least because assigning cache memory to one processor or another does not affect any relationship between different physical banks of memory. Additionally, the Examiner does not describe in the Office Action any facts or technical reasoning that would support the assertion of inherency. Moreover, the Office Action does not provide any extrinsic evidence to remedy this lack of rationale. In other words, the Examiner asserts the unsupported conclusion of

inherency in the Office Action, without providing any rationale or evidence to show how the Examiner necessarily would have arrived at the asserted conclusion of inherency.

Moreover, the further explanation provided by the Examiner in the Advisory Action also fails to support the assertion of inherency regarding remapping means and remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules, as recited in the claim. In the Advisory Action, the Examiner states:

> Regarding the limitation "to remap memory modules from a first physical bank of memory modules to a second physical bank of memory modules", during the switching of modes from two independent 2-way set associative caches to a single 4-way set associative cache (described at Column 7 Lines 11-30, also Column 7 Lines 64 to Column 8 Line 4), the physical banks of the SRAM of cache memory 23b are remapped from a 2-way set associative cache to part of a 4-way set associative cache. For example, data used by CPU 21a that could only be written to cache 23a (a first bank of memory modules) during the independent mode can be written to cache 23b (as second bank of memory modules) during 4-way set associative cache mode, satisfying the limitation of remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules.
>
> Advisory Action, 5/13/09, page 2, lines 7-14 (emphasis added).

Like the description of Cherabuddi referenced in the Office Action, this reasoning merely relates to assigning portions of a cache to the same or different processors. However, as explained above, assigning cache memory to different processors does not involve remapping memory modules from one physical bank to another. More specifically, reassigning cache memory from one processor to another does not involve remapping memory modules from one physical bank to another because Cherabuddi merely concerns how the cache memory is assigned to processors, but not how portions of the cache memory might relate to each other. In other words, Cherabuddi merely deals with whether cache memory is used jointly or separately by one or more processors. Thus, the Examiner's reasoning present in the Advisory Action does not add any additional rational or evidence in support of the assertion of inherency set forth in the Office Action mailed February 27, 2007.

Consequently, the description of separately using or jointly sharing the cache memory as described in Cherabuddi does not require that the missing disclosure of remapping memory modules from one physical bank to another would be necessarily present in the separate or combined use of the cache memory. Furthermore, the Examiner does not provide any explanation to show how the description of separately using or jointly sharing the cache memory necessarily would be recognized by a person of ordinary skill as inherently disclosing remapping memory modules from one physical bank to another. Additionally, even if it were possible to implement remapping memory modules from one physical bank to another, as recited in the claims of the present application, within the multiprocessor computer system of Cherabuddi, the mere possibility that remapping might be used in addition to the separate use or joint sharing of cache memory would not be sufficient to establish inherency.

Therefore, the rejection of claim 1 based on the purportedly inherent disclosure of remapping means is improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. In particular, neither the explanations in the Office Action mailed February 27, 2009, nor the further reasoning presented in the Advisory Action mailed May 13, 2009, provides evidence that assigning cache memory to one or more processors would necessitate remapping memory modules from one physical bank of memory to another physical bank of memory. Accordingly, the rejection of claim 1 is improper to the extent that the Examiner improperly relies on purported inherent disclosure that is not properly supported by rationale and evidence as required in the MPEP.

Appellants respectfully assert independent claim 8 is also patentable over Cherabuddi at least for one or more similar reasons to those stated above in regard to the rejection of independent claim 1. Although the language of claim 8 differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Appellants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 8. Accordingly, Appellants respectfully assert independent claim 8 is patentable over Cherabuddi at least because Cherabuddi does not disclose the indicated limitations.

Given that claims 2-7 and 9-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8, which are patentable over the cited reference, Appellants respectfully submit that dependent claims 2-7 and 9-20 are also patentable over the cited reference based on allowable base claims. Additionally, each of claims 2-7 and 9-20 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 1-20 under 35 U.S.C. 102(b) be withdrawn.

2. Cherabuddi does not disclose remapping means for remapping memory modules from a first physical bank of memory modules to a second physical bank of memory modules.

To the extent that the Examiner relies on the explicit disclosure of Cherabuddi, rather than the purportedly inherent disclosure, to show the remapping means as recited in the claim, the rejection nevertheless is improper because Cherabuddi does not explicitly disclose remapping means for remapping memory modules from one physical bank of memory to another physical bank of memory. As explained above, the explicit disclosure of Cherabuddi merely relates to a multiprocessor computer system partitions a cache memory depending on how many processors might be allowed to use or share the cache memory. In particular, the cache access circuit of Cherabuddi dynamically allocates the cache resources (i.e., the first and second cache memory partitions) between the first and second processors according to each processor's processing requirements. However, the description of separately using or jointly sharing the cache memory does not explicitly disclose remapping memory modules from one physical bank of memory to another physical bank of memory.

For the reasons presented above, Cherabuddi does not disclose all of the limitations of the claim because Cherabuddi does not disclose remapping means for remapping memory modules from one physical bank of memory to another physical bank of memory, as recited in the claim. Accordingly, Appellants respectfully assert claim 1 is patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claim.

Appellants respectfully assert independent claim 8 is also patentable over Cherabuddi at least for one or more similar reasons to those stated above in regard to the

rejection of independent claim 1. Although the language of claim 8 differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Appellants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 8. Accordingly, Appellants respectfully assert independent claim 8 is patentable over Cherabuddi at least because Cherabuddi does not disclose the indicated limitations.

Given that claims 2-7 and 9-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8, which are patentable over the cited reference, Appellants respectfully submit that dependent claims 2-7 and 9-20 are also patentable over the cited reference based on allowable base claims. Additionally, each of claims 2-7 and 9-20 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 1-20 under 35 U.S.C. 102(b) be withdrawn.

B. Claim 7 is patentable over of Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims.

Appellants respectfully submit that claim 7 is patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claim. Claim 7 recites:

> The integrated circuit according to claim 5, further comprising:
> a look up table for marking faulty memory modules.
> (Emphasis added.)

In support of the rejection of claim 7, the Examiner states:

> Regarding Claim 7, Cherabuddi teaches all limitations of Claim 5, further comprising a look up table for marking faulty memory modules (Column 9 Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty module.
> Office Action, 2/27/09, page 4 (emphasis added).

However, Cherabuddi does not teach the indicated limitation. In fact, the Examiner recognizes in the rejection of claim 15 that Cherabuddi does not teach marking faulty memory modules in a lookup table. Office Action, 2/27/09, page 12. Moreover, the portion (col. 9, lines 9-11) of Cherabuddi cited in the Office Action merely relates to

operating the cache memory partitions as 2-way and 4-way associative cache memories. But the cited portion does not disclose or address any type of lookup table. Therefore, Cherabuddi does not disclose a look up table for marking faulty memory modules.

For the reasons presented above, Cherabuddi does not disclose all of the limitations of the claim because Cherabuddi does not disclose a look up table for marking faulty memory modules, as recited in the claim. Accordingly, Appellants respectfully assert claim 7 is patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claim. Thus, Appellants request that the rejection of claim 7 under 35 U.S.C. 102(b) be withdrawn.

C. Claims 13 and 17 are patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims.

Appellants respectfully submit that claims 13 and 17 are patentable over Cherabuddi because Cherabuddi does not disclose all of the limitations of the claims. Claim 13 recites:

> The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.
> (Emphasis added.)

Claim 17 recites similar limitations. In support of the rejections of claims 13 and 17, the Examiner relies on conclusions of inherency in the Office Action. It is unclear from the explanations provided in the Advisory Action whether the Examiner continues to rely on inherency as the basis for the disclosure of the indicated limitations. Nevertheless, to the extent that the Examiner might rely on the purportedly inherent disclosure of Cherabuddi, Appellants maintain that such reliance on inherency is improper because the Examiner does not provide rationale or evidence to support the assertion of inherency.

In further addressing the indicated limitations, the Examiner states in the Advisory Action that:

> The cache modules of 23b are mapped from a 2-way set-associative cache to a 4-way set associative cache (described at Column 7 Lines 11-30, also Column 7 Line 64 to Column 8 Line 4), therefore what used to be the first and second ways of a 2-way set associative cache are remapped to the third and fourth ways of the 4-way set associate cache. One of ordinary skill in the art could reasonably assume that caches 23a and 23b are the same size and constructed in the same way, which keeps the indices the same after the transition from a 2-way set associative cache to a 4-way set associative cache.
>
> Advisory Action, 5/13/09, page 2 (emphasis added).

While the Examiner concludes a substantial amount of information from the cited portions of Cherabuddi, the actual disclosure of Cherabuddi does not support these conclusions. Moreover, there is no evidence to support the assertion of what one skilled in the art "could reasonably assume." Rather, the Examiner's statements merely form conjectures that are not supported by rationale or evidence because there is no explanation as to why one skilled in the art might reasonably assume the assertions presented by the Examiner.

Moreover, to the extent that the Examiner asserts these conclusions in support of the assertion of inherency, the assertion of inherency is nevertheless improper because the presumption of what one skilled in the art "could reasonably assume" is insufficient to show how the general description of transitioning between 2-way and 4-way set associative caches necessitates remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules. In other words, the possibility that one skilled in the art could make the asserted conclusion is insufficient to show how the description of Cherabuddi would necessarily require disclosure of the indicated limitations. Thus, the mere possibility that remapping might be used within the transition between 2-way and 4-way set associative caches is insufficient to establish inherency because the Examiner does not establish how transitioning between 2-way and 4-way set associative caches would necessitate such remapping.

Therefore, the rejections of claims 13 and 17 based on the purportedly inherent disclosure of Cherabuddi are improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. In particular, neither the

explanations in the Office Action mailed February 27, 2009, nor the further reasoning presented in the Advisory Action mailed May 13, 2009, provides evidence that transitioning between 2-way and 4-way set associative caches would necessitate remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules. Accordingly, the rejections of claims 13 and 17 are improper to the extent that the Examiner improperly relies on purported inherent disclosure that is not properly supported by rationale and evidence as required in the MPEP. Accordingly, Appellants request that the rejections of claims 13 and 17 under 35 U.S.C. 102(b) be withdrawn.

D. Claims 11 and 18 are patentable over the combination of Cherabuddi and Asher because the combination of cited references does not teach all of the limitations of the claims.

Appellants respectfully submit that claims 11 and 18 are patentable over the combination of Cherabuddi and Asher because the combination of cited references does not teach all of the limitations of the claims. Claim 11 recites:

> The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules. (Emphasis added.)

Claim 18 recites similar limitations. For clarification, the Examiner refers to Cherabuddi as purportedly teaching the indicated limitations of remapping to a new way, and the Examiner separately relies on Asher as purportedly teaching remapping to a different index. The Examiner's remarks in the Advisory Action are merely directed to the teachings of Asher. However, the Examiner's remarks in the Advisory Action do not address the purported teachings of Cherabuddi regarding remapping to a new way. Hence, the only reasoning presented by the Examiner regarding remapping to a new way is in the Office Action.

Although the Examiner states in the Office Action that remapping memory modules to a new way is purportedly inherent in the disclosure of Cherabuddi, the

Examiner's reliance on inherency is improper because the Examiner does not provide rationale or evidence to support the assertion of inherency. In particular, the Examiner's reliance on inherence is improper at least for similar reasons as explained above with general reference to the rejections of claims 13 and 17. As explained above, the Examiner's reasoning is insufficient to show how the general description of transitioning between 2-way and 4-way set associative caches necessitates remapping at least one of the memory modules to a new way within the second physical bank of memory modules. In other words, the possibility that one skilled in the art could make the asserted conclusion is insufficient to show how the description of Cherabuddi would necessarily require disclosure of the indicated limitations. Thus, the mere possibility that remapping might be used within the transition between 2-way and 4-way set associative caches is insufficient to establish inherency because the Examiner does not establish how transitioning between 2-way and 4-way set associative caches would necessitate such remapping.

Therefore, the rejections of claims 11 and 18 based on the purportedly inherent disclosure of Cherabuddi are improper because the assertion of inherency is not properly supported by rationale or evidence as required by the MPEP. In particular, neither the explanations in the Office Action mailed February 27, 2009, nor the further reasoning presented in the Advisory Action mailed May 13, 2009, provides evidence that transitioning between 2-way and 4-way set associative caches would necessitate remapping at least one of the memory modules to a new way within the second physical bank of memory modules. Accordingly, the rejections of claims 11 and 18 are improper to the extent that the Examiner improperly relies on purported inherent disclosure that is not properly supported by rationale and evidence as required in the MPEP. Accordingly, Appellants request that the rejections of claims 11 and 18 under 35 U.S.C. 103(a) be withdrawn.

E. Claims 3, 9, and 10 are patentable over the combination of Cherabuddi and Asher because the combination of cited references does not teach all of the limitations of the claims.

Claims 3, 9, and 10 depend from and incorporates all of the limitations of the corresponding independent claim 1. Appellants respectfully submit that dependent claims 3, 9, and 10 are also patentable over the combination of cited references based on an allowable base claim. Additionally, each of claims 3, 9, and 10 may be allowable for further reasons. Accordingly, Appellants request that the rejections of claims 3, 9, and 10 under 35 U.S.C. 103(a) be withdrawn.

F. Claim 6 is patentable over the combination of Cherabuddi and Kramer because the combination of cited references does not teach all of the limitations of the claim.

Claim 6 depends from and incorporates all of the limitations of the corresponding independent claim 1. Appellants respectfully submit that dependent claim 6 is also patentable over the combination of cited references based on an allowable base claim. Additionally, claim 6 may be allowable for further reasons. Accordingly, Appellants request that the rejection of claim 6 under 35 U.S.C. 103(a) be withdrawn.

G. Claims 12, 16, 19, and 20 are patentable over the combination of Cherabuddi and Supnik because the combination of cited references does not teach all of the limitations of the claim.

Claims 12, 16, 19, and 20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8. Appellants respectfully submit that dependent claim 12, 16, 19, and 20 are also patentable over the combination of cited references based on allowable base claims. Additionally, claims 12, 16, 19, and 20 may be allowable for further reasons. Accordingly, Appellants request that the rejection of claims 12, 16, 19, and 20 under 35 U.S.C. 103(a) be withdrawn.

H. Claim 15 is patentable over the combination of Cherabuddi and Emma because the combination of cited references does not teach all of the limitations of the claim.

Claim 15 depends from and incorporates all of the limitations of the corresponding independent claim 8. Appellants respectfully submit that dependent claim 15 is also patentable over the combination of cited references based on an allowable base claim. Additionally, claim 15 may be allowable for further reasons. Accordingly, Appellants request that the rejection of claim 15 under 35 U.S.C. 103(a) be withdrawn.

VIII. CONCLUSION

For the reasons stated above, claims 1-20 are patentable over the cited references. Thus, the rejections of claims 1-20 should be withdrawn. Appellants respectfully request that the Board reverse the rejections of claims 1-20 under 35 U.S.C. §§ 102 (b) and 103(a) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-20.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. An integrated circuit, comprising:

at least one processing unit (PU);

a cache memory (L2_bank) having a plurality of memory modules for caching data, wherein the cache memory comprises a plurality of distinct physical banks, wherein each physical bank comprises some of the memory modules and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks;

remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules.

2. The integrated circuit according to claim 1, wherein said cache memory (L2_BANK) is a set-associative cache.

3. The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.

4. The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols.

5. The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM).

6. The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM).

7. (previously presented) The integrated circuit according to claim 5, further comprising:

a look up table for marking faulty memory modules.

8. (previously presented) A method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing data; and a cache memory (L2_BANK) having a plurality of memory modules for caching data, the method comprising:

performing an unrestricted remapping within said plurality of memory modules, wherein the memory modules are distributed among a plurality of distinct physical banks within the cache memory, and each physical bank is configured to facilitate serving a read/write request independently of the other physical banks to allow concurrent transfers for at least two of the physical banks, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules.

9. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to distribute faulty memory modules evenly over a plurality of banks.

10. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to perform the unrestricted remapping at a block/line granularity of the memory modules.

11. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules.

12. (previously presented) The integrated circuit according to claim 1, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

13. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

14. (previously presented) The method of cache remapping according to claim 8, further comprising performing the unrestricted remapping on the basis of a reduction mapping using less output symbols than input symbols.

15. (previously presented) The method of cache remapping according to claim 8, further comprising marking faulty memory modules in a look up table.

16. (previously presented) The method of cache remapping according to claim 8, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

17. (previously presented) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

18. (previously presented) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a different index within the second physical bank of memory modules.

19. (previously presented) The integrated circuit according to claim 1, wherein each physical bank of memory modules is located on a separate DRAM module.

20. (previously presented) The method of cache remapping according to claim 8, wherein each physical bank of memory modules is located on a separate DRAM module.

X. EVIDENCE APPENDIX

There is no evidence submitted with this Appeal Brief.

XI. RELATED PROCEEDINGS APPENDIX

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.